WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first circuit composed of at least one MOS transistor;

a second circuit for controlling the frequency of a clock signal to be supplied to said first circuit;

a third circuit for controlling the voltage supplied to said first circuit;

a fourth circuit for controlling the substrate bias supplied to the semiconductor region where the MOS transistor of said first circuit is formed; and

wherein said clock signal frequency, said supply voltage and said substrate bias is adjusted according to the operating performance of said first circuit.

2. A semiconductor integrated circuit device as claimed in claim 1, further comprising:

a command generating circuit for controlling said clock frequency controlling circuit, said third circuit and said fourth circuit; and

wherein said command generating circuit generates a first, second and a third command signals according to said operating performance,

said second circuit sets a frequency of said clock signal in response to said first command signal,

said third circuit sets a value of said supply voltage in response to said second command signal, and

said fourth circuit sets a voltage value of said substrate bias in response to said third command signal.

3. A semiconductor integrated circuit device as claimed in claim 1, further comprising:

a command generating circuit for generating a first command according to said operating performance; and

a temperature compensation circuit for measuring a temperature of said main circuit; and

wherein said temperature compensation circuit issues second to fourth command signals according to said first instruction and the measured temperature of said first circuit,

said second circuit sets a frequency of said clock signal in response to said second command signal,

said third circuit sets a value of said supply voltage in response to said third command signal, and

said fourth circuit sets a voltage value of said substrate bias in response to said fourth command signal.

4. A semiconductor integrated circuit device as claimed in claim 1, wherein said operating performance includes at least an operating speed and a power

consumption of said first circuit,

at least one of the three parameters of said clock signal frequency, said supply voltage value and said substrate bias voltage is set in order to meet the operating speed, and

if the operating performance of said first circuit is changed from the first to the second state by controlling the other two or another parameter of said three parameters, said power consumption in the second state is smaller than that in the first state.

5. A semiconductor integrated circuit device as claimed in claim 1, wherein said operating performance includes at least an operating speed and a power consumption of said first circuit,

at least one of the three parameters of said clock signal frequency, said supply voltage value and said substrate bias voltage is set in order to meet the power consumption, and

if the operating performance of said first circuit is changed from the first state to the second state by controlling the other two or another one of said three parameters, said operating speed in the second state is faster than that in the first state.

6. A semiconductor integrated circuit device as claimed in claim 4, wherein said power consumption is controlled according to the remaining quantity of the battery for feeding an electric power to said semiconductor integrated circuit.

7. A semiconductor integrated circuit device as claimed in claim 2, wherein said command signal generated by said command generating circuit is determined according to at least one of a command from an operating system, a command from an application software, a signal input from the external, a signal from a memory or the processing load of said first circuit.

8. A semiconductor integrated circuit device as claimed in claim 2, wherein at least one of said command generating circuit, said second circuit, said third circuit, and said fourth circuit is formed on another chip rather than the chip where said first circuit is formed.

9. A semiconductor integrated circuit device comprising:

a first circuit composed of at least one MOS transistor;

a monitor composed of at least one MOS transistor;

a second circuit for controlling the frequency of a clock signal to be supplied to said first circuit;

a third circuit for controlling a supply voltage supplied to said first circuit;

a fourth circuit for controlling the substrate bias supplied to the semiconductor region where the MOS transistor of said first circuit is

formed; and

wherein any two of three parameters of said clock signal frequency, said supply voltage value and said substrate bias voltage value is set in order to meet the operating performance of said first circuit,

said clock signal, said supply voltage and said substrate bias are supplied to said monitor, and

the other ones of said three parameters is controlled so as to reduce a delay between the output of said monitor and a reference signal.

10. A semiconductor integrated circuit device as claimed in claim 9, wherein said monitor is a delay circuit composed of inverters connected in series, and further comprising a comparator for comparing an output of said monitor with said reference signal and outputting a first signal if the output of said monitor is later than said reference signal or a second signal if said reference signal is later than the output of said monitor, and wherein if said first signal is outputted, the other parameter is controlled so that the operating speed of said first circuit is made faster and if said second signal is outputted, the other parameter is controlled so that the operating speed of said first circuit is made lower.

11. A semiconductor integrated circuit device as claimed in claim 9, further comprising a command generating circuit for controlling the corresponding controls to said two parameters from said second

circuit, said third circuit, and said fourth circuit; and

wherein said command generating circuit generates a first and a second command signal according to said operating performance and the corresponding control circuits to said two parameters set their parameters in response to said first and second command signals.

12. A semiconductor integrated circuit device as claimed in claim 9, wherein said command signal generated by said command generating circuit is determined according to at least one of a command from an operating system, a command from an application software, a signal input from the external, a signal from a memory or a processing load of said main circuit.

13. A semiconductor integrated circuit device comprising:

a first circuit having a first conduction type first MOS transistor and a second conduction type second MOS transistor connected in series with said first MOS transistor; and

a second circuit for controlling the substrate bias supplied to the semiconductor region where said first and second MOS transistors are formed; and

wherein said second circuit suppresses variations of an operating frequency of said first

circuit by applying said substrate bias, and the frequency of a clock signal to be supplied to said first circuit and a supply voltage supplied to said first circuit are controlled against said first circuit whose operating frequency variations are suppressed.

14. A semiconductor integrated circuit device as claimed in claim 13, wherein said second circuit applies said substrate bias to said semiconductor region in the range from the forward bias to the back bias.

15. A semiconductor integrated circuit device as claimed in claim 13, wherein a first conduction type first well and a second conduction type second well are formed on a first conduction type substrate through a second conduction type isolation layer laid therebetween and said second MOS transistor is formed in said first well and said first MOS transistor is formed in said second well.

16. A semiconductor integrated circuit device as claimed in claim 13, wherein a first conduction type first well and a second conduction type second well are formed on said first conduction type substrate through an insulation layer laid therebetween, and said second MOS transistor is formed in said first well and said first MOS transistor is formed in said second well.

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